Rohan Gangaraju

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Education

Purdue University   **West Lafayette, IN**
Bachelor of Science in Computer Engineering   August 2020 - May 2024
- <u>Courses</u> - Compilers, Computer Architecture, Microprocessor and Systems, ASIC Design
- <u>Authorship</u> - *"Targeted Control-flow Transformations for Mitigating Path Explosion in Dynamic Symbolic Execution"* C. Saumya, **R. Gangaraju**, K. Sundararajah, and M. Kulkarni   **KLEE Workshop, CC 2024**

Skills

Languages: C, C++, Python, SystemVerilog, Java   **Tools:** Cadence Xcelium, Intel Quartas, NSight Compute
APIs: LLVM, CUDA, OptiX, Pandas   **Other:** UVM, RTL Design, FPGA, SoC Design

Research Experience

High Performance Compute Student Research Assistant, PurPL Lab   **West Lafayette, IN**
Mentors: Vani Nagarajan, Kirshanthan Sundararajah, Milind Kulkarni   May 2023 – Present
- Worked with **NVIDIA Ray Tracing (RT) Cores** in GPUs to accelerate diverse general-purpose computations
- Developed solutions using **C++**, **CUDA**, **OptiX** for mapping tree-traversals in n-body problems to RT Cores
- Profiled applications using **Nsight Compute/Systems** to identify bottlenecks and maximize throughput
- Acquired deep knowledge of **GPU architecture** and **parallel programming** principles

Compilers Undergraduate Research Assistant, PurPL Lab   **West Lafayette, IN**
Mentors: Charitha Saumya, Kirshanthan Sundararajah, Milind Kulkarni   October 2022 – May 2023
- Worked on compiler optimizations in **LLVM** to mitigate path explosion in **dynamic symbolic execution engines**
- Modified our LLVM pass to encode source-level debug information per line to perform **coverage analysis**
- Designed overarching iterative driver in **Python** to undo false-positive bugs introduced by our optimization

RISC-V CPU RTL Design Member, System on Chip Design (SoCET) Group   **West Lafayette, IN**
Mentors: Cole Nelson, Mark Johnson   January 2023 – Present
- Designed **SystemVerilog** modules to add **hardware multithreading** support to **RISC-V** based **microcontroller**
- Wrote module and system level testbenches in **C++** using **Verilator** to verify functionality
- Awarded **2nd Place** for research talk at *Purdue Fall 2023 Undergraduate Research Conference*

Project Experience

5-Stage Dual-Core MIPS Processor   Computer Architecture **(ECE 437)**
- Designed **MIPS** ISA-based **multicore processor** with 5-stage pipeline, hazard, forwarding units, and split caches
- Implemented **MSI protocol**-based bus controller for **dual-core coherence** + added **LL/SC synchronization** support
- Synthesized using **Intel Quartas Prime** onto Altera DE2-115 FPGA to benchmark clock speed and area utilization

Industry Experience

Software Engineering Intern   **Annapolis, MD**
Collins Aerospace, Raytheon Technologies   May 2022 – August 2022
- Developed and launched aircraft radio frequency mapping GUI tool using **Python**, **Leaflet**, and **PyQt**
- Developed **automatic coverage overlap process** using **Mapbox** and **ARCGIS** improving efficiency by over 70%

Embedded Software Engineering Intern   **Louisville, KY**
GE Appliances, A Haier Company   January 2022 – May 2022
- Remodeled software in refrigerator motherboards to support Smart Home and **IoT** technologies using **C and Lua**
- Implemented a **sensor filtering algorithm** to acquire optimum temperature and humidity readings